REMARKS

The Office Action dated June 27, 2003 has been received and carefully noted. The above amendments and the following remarks are submitted as a full and complete response thereto. Accordingly, claims 1-7 are pending in this application and are submitted for consideration.

Entry of this Amendment is proper under 37 C.F.R. § 1.116 since this Amendment: (a) places the application in condition for allowance for reasons discussed herein; (b) does not raise any new issue regarding further search and/or consideration since the Amendment amplifies issues previously discussed throughout prosecution; (c) does not present any additional claims without canceling a corresponding number of finally-rejected claims and (d) places the application in better form for appeal, should an appeal be necessary. The Amendment is necessary because it is made in reply to arguments raised in the rejection. Entry of the Amendment is thus respectfully requested.

Claim 1 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamamoto et al. (JP410144938A, "Yamamoto") in view of Kobayashi et al. (U.S. Patent No. 5,973,359 "Kobayashi"). In making this rejection, the Office Action took the position that Yamamoto discloses all the elements of the claimed invention, except for disclosing that the transistor comprises a plurality of transistor cells. Kobayashi is cited for curing the deficiencies of Yamamoto. However, Applicants respectfully traverse the rejection and submit that claim 1 recites subject matter that is neither disclosed nor suggested by any combination of the prior art.

Claim 1 recites a semiconductor device. This device includes an insulating gate field effect transistor. This transistor includes a plurality of transistor cells which are arranged in a semiconductor layer and connected in parallel. A protective diode is connected between a gate and a source of the insulating gate field effect transistor to break down an input of a constant voltage or more applied between the gate and the source. The protective diode is formed as a bidirectional diode in which one or more ring-shaped p-type layers and one or more ring-shaped n-type layers are flatly and alternately provided on an insulating layer at a peripheral portion than the transistor cells. Metal films in a ring-shape contacting with the most inner layer and the most outer layer of the p-type layers or the n-type layers are formed, respectively. Each of the metal films is successively formed with either a source wiring or a gate electrode pad consisting of a metal film, respectively.

This claimed configuration of the present invention provides a benefit and advantage because it improves the function of the protective diode by lowering the serial resistance of the protective diodes connected between a gate and a source of an insulating gate field effect transistor.

As discussed above, this invention includes (1) a protective diode that is mounted on the chip outer circumference (peripheral portion of a chip) to increase the area of the p-n junction, and (2) connections between the source electrode and the gate electrode on both end portions of the protective diode are brought in contact not with a semiconductor diffusion area or polysilicon film but with a ring-form metal film provided along the full circumferential length of the diode. An illustrative example of this configuration is provided in Figure 1(b) of the present specification. In Figure 1(b),

reference numeral 1 references the protective diode and reference numerals 2 and 3 represent the metal films.

Yamamoto discloses a ring-shaped metal film and also discloses bringing the layer on the innermost layer of the diode (n-layer) in contact with the metal film 16. However, Yamamoto does not disclose or suggest bringing the layer on the innermost layer and the outermost layer of the diode (n-layer) in contact with metal film. As clearly illustrated in Fig. 1(b) and Fig. 2(d), in Yamamoto, film 16 is located on an insulation film 15, and is not connected with outermost layer 12 of the sectional view.

As recited in the present claim 1, metal films in a ring-shape contact with the most inner layer and the most outer layer of the p-type layers or the n-type layers. This claimed configuration provides that benefit and advantage of bringing the metal film in contact almost throughout the full length of the outermost (most outer) layer. As shown in Fig. 1(a) of the present invention, unless the metal film (gate wiring 2) comes in contact almost throughout the full length of the layer, the resistance cannot be thoroughly lowered because the resistance of poly-silicon is excessively high.

Therefore, Yamamoto fails to disclose or suggest, metal films in a ring-shape contact with the most inner layer and the most outer layer of the p-type layers or the n-type layers, as recited in claim 1.

The Office Action admits that Yamamoto does not teach that the transistor is formed from a plurality of transistor cells. The Office Action cites Kobayashi as correcting this deficiency in Yamamoto. The Office Action took the position that one of ordinary skill in the art would be motivated to include the teaching of Kobayashi in the

invention taught by Yamamoto to reduce the area that is needed for protection of a multi-transistor-cell field, thereby reducing complexity and cost of the device.

While Kobayashi may disclose a plurality of transistor cells which are arranged in a semiconductor layer and connected in parallel, Kobayashi fails to correct the deficiencies discussed above in Yamamoto. Specifically, Kobayashi fails to show metal films in ring-shape contacting with the most inner layer and the most outer layer of the p-type layers or the n-type layers are formed, respectively.

Accordingly, the combination of Yamamoto and Kobayashi fails to teach and/or suggest the claimed invention. Specifically, the combination of these references fails to disclose and/or suggest metal films in ring-shape contacting with the most inner layer and the most outer layer of the p-type layers or the n-type layers are formed, respectively.

Therefore, it is respectfully submitted that the Applicants' invention, as set forth in claim 1, is not obvious within the meaning of 35 U.S.C. § 103.

Claims 1-6 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Williams et al. (U.S. Patent No. 6,268,242 B1, "Williams") in view of Yamamoto. In making this rejection, the Office Action took the position that Williams discloses all the elements of the claimed invention, except for disclosing that the metal film contacting the innermost and outermost layers is ring-shaped. Yamamoto is cited for teaching this limitation. However, the Applicants respectfully traverse the rejection and submit that claims 1-6 recite subject matter neither disclosed nor suggested by the prior art.

Williams discloses forming a diode around the gate pad described in Figure 9 of the present application. In this construction, the gate pad is connected directly to the

inner circumferential edge of the diode. The outer circumferential end of the diode is connected to the source wiring that is connected to the transistor cells located around the diode.

The Office Action admitted that Williams does not teach that the metal film contacting the innermost and outermost layers is ring-shaped. The Office Action, however, asserted that it would have been obvious to improve the invention of Williams to include such ring-shaped contacts in view of Yamamoto, since Yamamoto teaches forming the Zener diode in a ring-shape for the purpose of increasing the electrostatic strength of the Zener diode.

Williams, however, does not disclose that connecting both end portions of the diode with metal films reinforces the protective functions of the diode. Additionally, if the diode of Williams is formed into a ring form and positioned on the periphery of the integrated circuit, there would be no cell area around the outer circumference to form a cell area. Accordingly, it would not be obvious to one of ordinary skill in the art to convert the diode construction taught in Williams into a ring form.

In contrast, Yamamoto discloses increasing the protective function of the diode by increasing the area of the p-n junction. Yamamoto, however, does not teach and or suggest connecting the outermost layer of the diode with metal film for further lowering the serial resistance while providing a diode on the chip outer circumference. Further, as discussed above, Yamamoto does not disclose or suggest bringing the layer on the innermost layer and the outermost layer of the diode (n-layer) in contact with metal film.

Since Williams fails to teach and/or suggest that the protective function of the diode could be improved by use of metal films to connect both end portions of the diode,

it would not be obvious to combine Williams and Yamamoto since the conversion of the Zener diode shown in Williams to the ring-shaped Zener diode shown in Yamamoto would require the displacement of the transistor cells taught in Yamamoto, thereby changing the principle of operation of the references.

Furthermore, claim 3 recites in part, that the one ring-shaped metal film is a gate wiring which has gate connecting potions so as to connect to gate electrodes of the transistor cells with partial striding over the protective diode. Neither Williams, nor Yamamoto, either alone or in combination disclose or suggest this limitation. In the present invention, as a result of this claimed configuration, by connecting the metal film located on the chip outer circumference directly to the gate electrodes of transistor cells, the effect of transmitting signals without resistance loss to the whole transistor cells located on the whole chip can be achieved via the metal film.

Accordingly, Applicants respectfully request reconsideration and withdrawal of the rejection of claims 1-6 under 35 U.S.C. § 103(a).

Additionally, since claims 2-6 depends either directly or indirectly from claim 1, Applicants respectfully submit that each of these claims incorporates the patentable aspects of claim 1, and are therefore allowable, for at least the same reasons.

Claim 7 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Williams and Yamamoto, or in the alternative Yamamoto and Kobayashi as applied to claim 1, and further in view of Throngnumchai et al. (U.S. Patent No. 4,963,970, "Throngnumchai"). However, as will be discussed below, Applicants respectfully submit that the prior art, in any combination, fails to disclose or suggest the claimed invention.

Claim 7 recites a semiconductor device including an insulating gate field effect transistor having a plurality of transistor cells which are arranged in a semiconductor layer and connected in parallel. A protective diode is connected between a gate and a source of the insulating gate field effect transistor to break down an input of a constant voltage or more applied between the gate and the source. The protective diode is formed as a bidirectional diode in which one or more ring-shaped p-type layers and one or more ring-shaped n-type layers are alternately laminated in a height direction three or more layers on an insulating layer at a peripheral portion of the transistor cells. Ring-shaped metal films contact with the bottom layer and the top layer of the p-type layers or the n-type layers, and each of the metal films is successively formed with either of a source wiring or a gate electrode pad consisting of a metal film, respectively.

As discussed above, Yamamoto fails to disclose or suggest ring-shaped metal films in contact with the bottom layer and the top layer of the p-type layers or the n-type layers. The Office Action admits that Williams fails to disclose or suggest this feature.

Furthermore, with respect to claim 7, the present invention forms a bidirectional diode in the longitudinal direction using a lamination of three or more layers. The bottom layer and the top layer are brought into contact with the metal films. Throngnumchai, however, only discloses a two-layer construction. Accordingly, this reference fails to teach and/or suggest the invention recited in claim 7.

Therefore, Applicants respectfully request reconsideration and withdrawal of the rejection of claim 7 under 35 U.S.C. § 103(a).

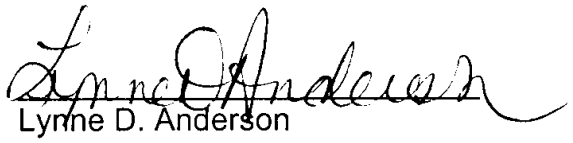
In view of the foregoing, reconsideration of the application, withdrawal of the outstanding rejections, allowance of claims 1-7, and the prompt issuance of a Notice of

Allowability are respectfully solicited.

If this application is not in condition for allowance, the Examiner is requested to contact the undersigned at the telephone listed below.

In the event this paper is not considered to be timely filed, the Applicants respectfully petition for an appropriate extension of time. Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300, **referencing docket number 107400-00044.**

Respectfully submitted,
ARENT FOX KINTNER PLOTKIN & KAHN PLLC



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